REMARKS/ARGUMENT

Claims 12-16 are allowed.

1) Claims 3-8, 18-19 and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Peterzell et al. (US 5,722,063). Applicants respectfully traverse this rejection as set forth below.

An obviousness inquiry is decided as a matter of law, based on four general factual inquiries as explained in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966), and reaffirmed in *KSR International, Inc. v. Teleflex, Inc.*, 550 U.S. 398, 406-07 (2007). The patent examiner is responsible for marshalling the references whose teachings are most relevant to the claimed invention, and evaluating the claimed invention against these teachings, from the viewpoint of a person of ordinary skill in the field of invention. See *Graham*, supra; *In re Kubin*, 561 F.3d 1351, 1355 (Fed. Cir. 2009); see generally *In re Oetiker*, 977 F.2d 1443, 1445-47 (Fed. Cir. 1992).

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

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Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." <u>In re Wilson</u>, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 5 requires and positively recites, an apparatus, comprising: "two or more adaptive equalizers", "a plurality of operation blocks that interconnect the adaptive equalizers", "a <u>first control mechanism</u> that <u>configures</u> the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles", "a second control mechanism that <u>disables</u> at least one of said plurality of operational blocks according to the different signal delay profiles" and "a <u>third control mechanism</u> that <u>disables</u> a computation resource of at least one of said adaptive equalizers according to the different delay profiles".

Independent Claim 8 requires and positively recites, an apparatus, comprising: "two or more adaptive equalizers", "a plurality of operation blocks that interconnect the adaptive equalizers", "a <u>first control mechanism</u> that <u>configures</u> the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles", "a second

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control mechanism that <u>disables</u> at least one of said plurality of operational blocks according to the different signal delay profiles" and "a <u>third control mechanism</u> that <u>disables</u> a computation resource of at least one of said adaptive equalizers according to the different delay profiles, the first, second, and third control mechanisms comprise multiplexers that receive control signal according to the different delay profiles".

In contrast, Ueda discloses an apparatus that "selects" between decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or between adaptive equalizer 180 and linear adaptive equalizer 181) in response to a signal delay profile. More particularly, Ueda teaches:

Based on the correlation value, the control signal output circuit makes a decision as to whether either one of the decision feedback adaptive equalizer 175 and the linear adaptive equalizer 176 should be operated with respect to its burst depending on the ratio of the value of the direct wave of the correlator to that of the delay wave thereof and the maximum delay time of the delay wave. As a criterion for this decision, there is a method of activating the linear adaptive equalizer 176 if the maximum delay time of the delay wave is less than or equal to 0.35 symbol and of activating the decision feedback adaptive equalizer 175 the maximum delay time is more than or equal to 0.35 symbol, both using the result of bit error rate performance shown in FIG. 2, for example. After the adaptive equalizer to be operated has been decided, the delay measuring circuit 174 outputs the control signal to the decision feedback adaptive equalizer 175 when the decision feedback adaptive circuit 175 is activated, whereas the delay measuring circuit 174 outputs the control signal to the linear adaptive equalizer 176 when the linear adaptive equalizer 176 is activated (col. 46, line 57 – col. 47, line 10).

In light of the above, there is selecting, but NO "configuring" of Ueda's decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or feedback adaptive equalizer 180 and linear adaptive equalizer 181), as suggested by Examiner. Accordingly, Ueda fails to teach or suggest, "a <u>first control mechanism</u> that <u>configures</u> the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles", as required by Claims 5 and 8.

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Examiner equates Ueda's "unique word 11" as being the equivalent to "first control mechanism" in Claims 5 & 8. However, Ueda confirms that UW 11 is a "unique word" (col. 2, lines 3-4) – NOT a "mechanism" (i.e., a system of parts). As such, Examiner's determination that Ueda teaches, "a <u>first control mechanism</u> that <u>configures</u> the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles", as required by Claims 5 and 8, is erroneous and must be withdrawn.

Next, Examiner equates Ueda's training of the equalizers for setting up the taps in the decision feedback adaptive equalizer 127 and 133 and the taps in the linear adaptive equalizer 130 and 136 based on the received unique word (UW) that indicate the propagation characteristic of channel, as shown in Figure 11 (which is embodiment seven of his invention (col. 33, line 66 – col. 34, line 5)) and column 35, lines 18-44 as being equivalent to "configures the adaptive equalizers and the plurality of operation blocks according to different signal delay profiles", as required by Claims 5 and 8 (OA, page 3, lines 8-11). Yet, it is not possible that a "word" configures anything. A "word" may be used to assist a mechanism to "configure" something, but a "word" in and of itself cannot. As such, Ueda fails to teach or suggest, "...that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles", as required by Claims 5 and 8.

Examiner next interprets comparator 124 outputting the result of selection to the selecting circuit 140 which outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, these adaptive equalizers tope the equalization of the remaining random data corresponding to the same burst in response to the stop signal (col. 36, lines 14-19), as being equivalent to "a **third control mechanism** that **disables a computation resource of at least one of said adaptive equalizers** according to the different delay profiles" (OA, page 3, line 21 – page 4, line 9).

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Applicants respectfully point out that comparator 124 and selecting circuit 125 are disclosed in Figure 10, which discloses a block diagram showing the structure of the sixth embodiment of Ueda's invention (col. 31, lines 21-22), while comparator 139 and selecting circuit 140 are disclosed in Figure 11, which discloses a block diagram showing the structure of the <u>seventh</u> embodiment of Ueda's invention (col. 33, line 66 – col. 34, line 1). Ueda specifically confirms that in the drawings, the same elements of structure as those employed in the convention example and the sixth embodiment are identified by the same reference numerals (col. 34, lines 1-5). Thus, the Examiner can not mix and match comparator 124 of Figure 10 with selecting circuit 140 of Figure 11 since there is no teaching or suggestion in Ueda that these two circuits can be combined. In short, Examiner is improperly assuming that Figures 10 & 11 of Ueda teach the same device, which in fact they do not since they are separate embodiments and Ueda specifically sets forth that to have the same function, a device will have the same reference number. Accordingly, Examiner's determination that Ueda teaches "a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different delay profiles", as required by Claims 5 & 8 is improper and must be withdrawn.

In addition to the above, Ueda teaches respective enabling of decision feed back adaptive equalizer 175 or linear adaptive equalizer 176 (and square error integrating circuit 182 selects between decision feed back adaptive equalizer 180 or linear adaptive equalizer 181), which also implies enabling of the computation resource within when an adaptive equalizer is selected. No where does Ueda teaches "disabling" of a computation resource in one of the adaptive equalizers "according to a different delay profile", as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Ueda fails to teach or suggest, "a **third control mechanism** that **disables** a **computation resource of at least one of said adaptive equalizers** according to the different delay profiles", as required by Claims 5 and 8.

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Examiner admits that Ueda fails to teach or suggest, "a second control mechanism that <u>disables</u> at least one <u>of said plurality of operational blocks according to the</u> <u>different signal delay profiles</u>", as required by Claims 5 and 8 (OA, page 4, lines 10-15). Examiner, however, now relies upon Peterzell as teaching to power down a device when the device is not in use (bypasses) by a controller in order to reduce power consumption (OA, page 4, lines 16-18). Ueda actually teaches the following:

In all of the above embodiments, the LNA can be powered down at the same time that it is bypassed by the switch or switches. This can be accomplished by connecting the LNA's power pin to a switch that is also controlled by the controller. Once the LNA is bypassed and is no longer used, power can be removed. This reduces the power consumption of the radio, thus increasing the talk and standby time for which the battery can be used (col. 7, lines 39-46).

Peterzell teaches disconnecting power of a LNA to reduce power consumption. Yet Ueda does not teach or suggest that an LNA, such as set forth in Peterzell is, or can be, one of its "operational blocks". Thus, Examiner's determination that Peterzell's teaching of disconnecting power of a LNA to reduce power consumption is, or can be, equated to a second control mechanism in Ueda to disable at least one of Ueda' plurality of operation blocks, is supposition not supported by fact. Indeed, little more than improper hindsight reconstruction.

In addition to the above, while Examiner determines that Peterzell teaches to power down a device when the device is not in use by a controller in order to reduce power consumption (OA, page 4, lines 16-18), Examiner fails to forth what he considers "the second control mechanism" in Peterzell. As such, Examiner has not considered ALL of the words of Claims 5 & 8, as is required by law. For this reason alone, the rejection of Claims 5 & 8 is improper and must be withdrawn.

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In yet addition to the above, even if, arguendo, Peterzell teaches disconnecting power of a LNA to reduce power consumption, there is no teaching or suggestion in Peterzell that power is disabled to its LNA "according to the different signal delay profiles". As such, Peterzell fails to teach or suggest, "a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles", as required by Claims 5 and 8.

But even if, arguendo, Peterzell were to teach what is suggested by Examiner, Peterzell fails to teach or suggest the remaining above-identified deficiencies of Ueda as applied to Claims 5 & 8. As such, any combination of Ueda and Peterzell fails to teach or suggest all of the limitations of Claims 5 & 8.

Thus, even if, arguendo, Ueda and Peterzell can be combined as suggested by Examiner, the resulting combination yet fails to teach or suggest the resulting combination and omits key limitations of Claims 5 & 8. "Skill in the art does not act as a bridge over gaps in the substantive presentation of an obviousness case, but instead supplies an important guarantee of objectivity in the process", Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001)(quoting Litton Industrial Prods., Inc. v. Solid State Systems Corp., 775 F.2d 158, 163 (Fed Cir. 1985). While KSR related some of the formalism of earlier decisions requiring a "teaching, suggestion, or motivation" to combine prior art references, it did not remove the need to anchor the analysis in explanation of how a person of ordinary skill would select and apply the teachings of the references. Obviousness is determined as a matter of foresight, not hindsight. See KSR at 421 (citing Graham, 383 U.S. at 36). KSR did not free the PTO's examination process from explaining its reasoning. In making an obviousness rejection, the examiner should not rely on conclusory statements that a particular feature of the invention would have been obvious or was well known. Instead, the examiner should elaborate, discussing the evidence or reasoning that leads the examiner to such a conclusion. Generally, the

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examiner cites prior art references to demonstrate the state of knowledge See <u>37 C.F.R. § 1.104(c)(2)</u> ("In rejecting claims for want of novelty or obviousness, the examiner must cite the best references at his or her command."); <u>Manual of Patent Examining Procedure (MPEP)</u> § 706.02 (8th ed., rev. July 2008). If an examiner is able to render a claim obvious simply by saying it is so, neither the Board of Appeals nor the Court of Appeals for the Federal Circuit is capable of reviewing that determination. <u>See KSR</u>, 550 U.S. at 418, <u>citing In re Kahn</u>, 441 F.3d 977, 988 (Fed. Cir. 2006)("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). Accordingly, the 35 U.S.C. 103(a) rejection of Claims 5 & 8 is improper and must be withdrawn.

Claims 3, 4, 6 and 7 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the apparatus of claim 5 wherein each of said two or more adaptive equalizers comprise a computational resource. Claims 3 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Claim 4 further defines the apparatus of claim 3 wherein the computation resource comprises at least one item selected from the group consisting of: a summer, a conjugation block, a multiplier, and a divider. Claims 4 stands allowable as depending from allowable Claim 3 and including further limitations not taught or suggested by the references of record.

Claim 6 further defines the apparatus of claim 5 wherein said operational blocks comprise at least one item selected from the group consisting of: "a signal regenerator", "a

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delay line" and "a summer". Accordingly, Claim 6 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Claim 7 further defines the apparatus of claim 5 wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of: "sub-signals that arrive to the apparatus in consecutive chip time unit", "sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals", "subsignals that do not arrive to the apparatus in consecutive chip time units", "sub-signals that arrive to the apparatus in two or more clusters" and "sub-signals that arrive to the apparatus from more than one antenna". Claims 7 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record. Moreover, Examiner cites no authority in Ueda that teaches or suggests "sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals". Examiner is silent. Further, while Ueda teaches that when a delay wave is less than or equal to 0.35 symbol linear adaptive equalizer 176 is selected, whereas if the maximum delay time of the delay wave is more than 0.35, then decision feedback adaptive equalizer 175 is selected (col. 46, line 63 – col. 47, line 3), Ueda does not further teach or suggest any "clusters" of signals as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Claim 7 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Independent 18 requires and positively recites, a system comprising: "two or more adaptive equalizers", "a plurality of operational blocks", "a means for <u>selectively</u> interconnecting the two or more adaptive equalizers and the plurality of operational <u>blocks</u> according to the attributes of a signal profile" and "a means for <u>disabling</u> a

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computation resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile, the means for selectively interconnecting and the means for disabling comprising a plurality of multiplexers".

In contrast, Ueda discloses an apparatus (selecting circuit 140) that "selects" between equalized-output memories 129, 132, 135, and 138. More particularly, Ueda teaches:

Reference numeral 140 indicates <u>a selecting circuit for selecting one of the equalized outputs</u> produced from the equalized-output memory 129, the equalized-output memory 132, the equalized-output memory 135 and the equalized-output memory 138 in accordance with the output control signal generated from the comparator 139 (col. 34, lines 49-55).

In light of the above, there is selecting, but NO "selective <u>interconnecting</u>" of equalized-output memories 129, 132, 135 and 138, as determined by Examiner. As such, Ueda fails to teach or suggest, "<u>selectively interconnecting the two or more adaptive</u> <u>equalizers and the plurality of operational blocks</u> <u>according to the attributes of a signal profile</u>", as required by Claim 18.

In addition to the above, Ueda teaches:

Thereafter, the comparator 124 outputs the result of selection to the selecting circuit 140 and outputs a stop signal to each of the remaining three *adaptive equalizers* which have not been selected (col. 36, lines 13-17).

There is no teaching whatsoever in the above that selecting circuit 140 further disables any of square error integrating circuits 128 and 134, square error integration circuit 131 and 137 or comparator 139 and selecting circuit 140, which Examiner equates to being "operational blocks". As such, Ueda fails to further teach or suggest, "a means for

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<u>disabling</u> a <u>computation resource of at least one of the two or more adaptive equalizers</u> according to said attributes of the signal profile ...", as further required by Claim 18.

Examiner admits that Ueda fails to teach or suggest, "means for selectively interconnecting and the means for disabling comprising a multiplexer" (OA, page 11, lines 20-21). Examiner, however, relies upon Peterzell as teaching a controller that is used in order to reduce power consumption by connecting a power pin to a switch that is also controlled by a controller and thereafter arguing that it is "inherent" that such a switch is equivalent to a multiplexer (OA, page 12, lines 1-5). Applicants traverse this determination.

Even if, arguendo, Peterzell teaches a controller that is used in order to reduce power consumption by connecting a power pin to a switch that is also controlled by a controller, as suggested by Examiner, there is no further teaching in Peterzell or knowledge available to one having ordinary skill in the art that would necessitate that such controller be a "multiplexer", as suggested by Examiner's "inherency" argument. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' ... 'Inherency however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient". *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Int'f 1990). "A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim."; "About the most that can be said for the [prior art] patent is that it does not explicitly describe anything inconsistent with [the claimed] procedures. However, this negative pregnant is no

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enough to show anticipation." *Rowe v. Dror*, 112 F.3d 473, 478, 480-81, 42 USPQ2d 1550, 1553, 1555 (Fed. Cir. 1997). Summary judgment of inherency anticipation was improper because of a material fact issue whether a prior art reference's process necessarily produced the claimed invention's features; "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill". *Continental Can Company USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1269, 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991). Examiner's argument does not meet the above criteria since Examiner has provided no evidence showing that Peterzell's controller IS, or must be, a multiplexer. As a result, Examiner's inherency argument is not supportable. Supposition not supported by fact simply can not be used to establish a prima facie case of obviousness.

Moreover, even if, arguendo, Peterzell has disclosed that the controller identified by Examiner was a "multiplexer", Peterzell fails to teach or suggest the previously identified deficiencies of Ueda, as applied to Claim 18. As a result, any combination of Ueda and Peterzell fails to teach or suggest all of the limitations of Claim 18.

Accordingly, the 35 U.S.C. 103(a) rejection of Claim 18 is improper and must be withdrawn.

Claims 19 and 22 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 19 further defines the system of claim 18 further comprising means for disabling at least one of the plurality of operational blocks according to said attributes of

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the signal profile. Claims 19 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record.

Claim 22 further defines the system of claim 18, wherein the attributes of the signal profile comprise at least one selected from the group consisting of: "a number of antennas that transmitted the multi-path signal", "a length of the multi-path signal profile", "an amount of energy in a single sub-signal of the multi-path signal", "an amount of capturable energy by a number of adaptive equalizers" and "a number of energy clusters". Claims 22 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record. Moreover, Examiner cites no authority in Ueda that teaches or suggests, "an amount of energy in a single subsignal of the multi-path signal", "an amount of capturable energy by a number of adaptive equalizers" and "a number of energy clusters" (OA, page 13, lines 10-12). Examiner is silent. Further, while Ueda teaches that when a delay wave is less than or equal to 0.35 symbol linear adaptive equalizer 176 is selected, whereas if the maximum delay time of the delay wave is more than 0.35, then decision feedback adaptive equalizer 175 is selected (col. 46, line 63 – col. 47, line 3), Ueda does not further teach or suggest any "amount of energy in any single sub-signal of the multi-path signal" or "an amount of capturable energy by any of the equalizers", or "number of energy clusters" as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Claim 22 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record.

3) Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Peterzell et al. (US 5,722,063) in view of Yang (US 6,763,074 B1). Applicants respectfully traverse this rejection as set forth below.

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Claim 9 further defines the apparatus of claim 5 wherein a two-stage configuration

of the apparatus comprises a default mode. Claim 9 stands allowable as depending from

allowable Claim 5 and including further limitations not taught or suggested by the

references of record. Moreover, even if, arguendo, Yang discloses wherein a two-stage

configuration of the apparatus comprises a default mode, as suggested by Examiner, Yang

fails to teach or suggest the above identified deficiencies of Ueda and Peterzell as applied to

Claim 5. Accordingly, any combination of Ueda, Peterzell and Yang fails to teach or

suggest all of the limitations of Claim 9, as is required by law. Accordingly, the 35 U.S.C.

103(a) rejection of Claim 9 is improper and must be withdrawn.

4) Claim 21 stands rejected under 35 U.S.C. 103(a) as being unpatentable over

Ueda (US 5,644,597) in view of Peterzell (US 5,722,063) as applied to claim 18 above, and

further in view of Juan (US 5,642,382). Applicants respectfully traverse this rejection as set

forth below.

Claim 21 further defines the system of Claim 18 by further comprising means for

sharing computational resources of the two or more adaptive equalizers. Claim 21 stands

allowable as depending from allowable Claim 18 and including further limitations not

taught or suggested by the references of record. Moreover, even if, arguendo, Juan discloses

a system that shares a single set of arithmetic operators between filters of the equalizers, as

suggested by Examiner, Juan fails to teach or suggest the above identified deficiencies of

Ueda as applied to Claim 18. Accordingly, any combination of Ueda, Peterzell and Juan

fails to teach or suggest all of the limitations of Claim 21, as is required by law.

Accordingly, the 35 U.S.C. 103(a) rejection of Claim 21 is improper and must be

withdrawn.

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Application No. 10/699,707 Amendment dated July 29, 2011

Reply to Office Action of May 24, 2010

Claims 12-16 are allowed. Claims 3-4, 5, 6-8, 9, 18, 19, 21-22 are allowable for

the reasons set forth above. Applicants appreciate Examiner's determination on page 15,

lines 3-5 that Claims 3-4, 6-7, 9, 19 and 21-22 are objected to as being dependent upon a

rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims. Claims 3-4, 6-7, 9, 19

and 21-22 have already been rewritten in independent form including all of the

limitations of the base claim and any intervening claims and thus stand allowable.

Applicants respectfully request withdrawal of the rejections and allowance of the

application as the earliest possible date.

Respectfully submitted,

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